ABSTRACT

Methods and apparatus are provided. A NAND memory array has a select line coupled to each of a plurality of NAND strings of memory cells of the memory array. The select line has a select gate at each intersection of one of the plurality of NAND strings and the select line. The select line further includes first and second conductive layers separated by a dielectric layer, and a contact that extends from a third conductive layer, disposed on the second conductive layer, to the first conductive layer. The contact is formed in a hole that passes through the second conductive layer and the dielectric layer and that terminates at the first conductive layer. The contact electrically connects the first and second conductive layers. The hole can have a slot shape so that the contact spans two or more NAND strings of the plurality of NAND strings.